	Application No.	Applicant(s)
Notice of Allowability	10/607,934	ANVIN, H. PETER
	Examiner	Art Unit
	Leonid Kravets	2189
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to <u>amendment filed 2/17/06</u> .		
2. The allowed claim(s) is/are 1,3,5-8,10,12-16 and 19-21.		
3.		
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/C Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview Summary Paper No./Mail Da 08), 7. ☑ Examiner's Amend	ite

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EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Glen Barnes (Reg No 42,293) on March 21, 2006.

2. The application has been amended as follows:

Amend Claim 1, Lines 9-11 to read "using a logical AND to combine a plurality of memory protection bits, wherein at least one of the memory protection bits is a dirty bit, for the plurality of TLB entries to enforce memory protection the virtual machine application"

Cancel claim 2

Amend Claim 8, Lines 15-17 to read "using a logical AND to combine a plurality of memory protection bits, wherein at least one of the memory protection bits is a dirty bit, for the plurality of TLB entries to enforce memory protection on the virtual machine application"

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Cancel claim 9

Amend Claim 15, Lines 11-13 to read "using a logical AND to combine a plurality of memory protection bits, wherein at least one of the memory protection bits is a read/write bit, for the plurality of TLB entries to enforce memory protection on the virtual machine application"

Cancel claim 17

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REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance: The independent claims 1 and 8, as amended by examiner's amendment are drawn to a method for providing hardware support for memory protection...using a logical AND to combine a plurality of memory protection bits, wherein at least one of the memory protection bits is a dirty bit. Similarly independent claim 15 as amended requires a read/write bit to be used in a logical AND operation to enforce memory protection on the virtual machine application.

Examiner was unable to find prior art anticipating the independent claims, further no references when combined obviated or gave sufficient motivation for using a dirty bit or read/write bit in a logical AND operation to enforce memory protection on the virtual machine application.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on Mon-Fri 8-430.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonid Kravets Patent Examiner Art Unit 2189

REGINALD G. BRAGDON PRIMARY EXAMINER

Regural & Bragain

April 13, 2006